

DEC 15 2005

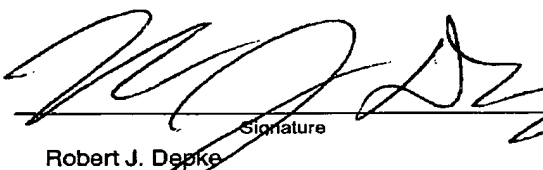
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PRE-APPEAL BRIEF REQUEST FOR REVIEW		Docket Number (Optional) 075834.00038	
I hereby certify that this correspondence is being facsimile transmitted to the Patent and Trademark Office to fax number (571) 273-8300. on <u>12/15/05</u> Signature <u>[Signature]</u> Typed or printed name <u>Robert J. Depke</u>		Application Number 09/447,301	Filed November 23, 1999
		First Named Inventor Satoshi Yoshihara	
		Art Unit 2612	Examiner James A. Hannett
<p>Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.</p> <p>This request is being filed with a notice of appeal.</p> <p>The review is requested for the reason(s) stated on the attached sheet(s). Note: No more than five (5) pages may be provided.</p> <p>I am the</p> <p><input type="checkbox"/> applicant/inventor.</p> <p><input type="checkbox"/> assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)</p> <p><input checked="" type="checkbox"/> attorney or agent of record. 37,607 Registration number _____</p> <p><input type="checkbox"/> attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____</p> <p>NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.</p> <p><input type="checkbox"/> *Total of _____ forms are submitted.</p>			



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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.: 09/447,301 **Confirmation No.:** 3648
Applicant: Satoshi Yoshihara
Filed: November 23, 1999
TC/A.U.: 2612
Examiner: James M. Hannett
Docket No.: 075834.00038
Customer No.: 33448

PRE-APPEAL BRIEF REQUEST FOR REVIEW ACCOMPANYING

NOTICE OF APPEAL

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S I R:

ERRORS IN THE PRIOR REJECTION

Consistent with the Review Requirements for identification of clear errors, Applicants note the following:

- I. The prior art fails to anticipate at least the limitation that the solid-state image-pickup device includes a plurality of transfer registers wherein said plurality includes two transfer registers which receive and concurrently transfer signal charges from at least two rows of pixels of said sensor array.
- II. The prior art fails to teach or suggest at least the limitation that the solid-state image-pickup device includes a plurality of transfer registers wherein said plurality includes two transfer registers which receive and concurrently transfer signal charges from at least two rows of pixels of said sensor array.

REMARKS**A. The §102 Prior Art Rejection Is Improper**

Applicants respectfully request reconsideration of the Examiner's rejection of claims 1 – 8, 11, and 12 under 35 U.S.C. §102(b). Examiner has rejected these claims in view of the cited prior art reference of *Elabd et al.* (U.S. Patent No. 5,196,939).

“A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.” *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

In the April 20, 2005 Amendment, Applicants added the further limitation that the solid-state image pickup device of the instant invention include two transfer registers which receive and concurrently transfer signal charges from at least two rows of pixels of said sensor array. The asserted *Elabd* reference only discloses the concurrent transfer of **one** row of pixels concurrently in two horizontal transfer registers (even and odd pixels of a single row are transferred to respective horizontal transfer registers and driven out).

In the Office Action mailed on July 15, 2005, in apparent acknowledgement of the failed teachings of the *Elabd* reference, the Examiner took the position that the image sensor configuration in Figure 4 of *Elabd* can “be rotated 90 degrees counter clockwise so the transfer registers are located to the left of the image sensor and therefore, each transfer register collects data from a plurality of **rows** of image data instead of a plurality of **columns**

as would be the case if the paper was oriented to have the transfer registers depicted at the top of the page.” Applicants respectfully reject the propriety of the Examiner’s position.

As noted above, the Federal Circuit has made clear that the prior art in a §102 rejection must teach *each and every element* of the claimed invention. Here, the Examiner continues to assert a §102 rejection, while simultaneously acknowledging that the *Elabd* reference fails to disclose a significant claim limitation.

Furthermore, Applicants submit that “row” and “column” are terms of art used in the field of semiconductor imaging products and methods. Applicants certainly agree that the image sensor array 13 in Figure 4 of *Elabd* can be rotated 90 degrees clockwise or counterclockwise. However, Applicants submit that the definition of “row” and “column” would change accordingly. More specifically, “row” and “column” are defined in reference to the Vertical Transfer Registers 15 and the Horizontal Transfer Registers 17A and 17B. As stated in Column 4, lines 33 – 34 of the *Elabd* reference, “A group of vertical registers 15 are used to transfer rows of data held in image array 13 to storage register 33.” (Emphasis added). Accordingly, no matter how the image sensor is rotated in Figure 4, one of ordinary skill in the art would still view the vertical transfer registers 15 as transferring rows of image data. That is the ordinary and customary use of the terms in the art, in the *Elabd* reference, and in Applicant’s own specification.

The Examiner cannot construe the terms “row” and “column” counter to how Applicant’s have defined and used the terms, and counter to the accepted use in the art of semiconductor imaging devices, in order to defeat patentability.

In light of the foregoing, it becomes even clearer that *Elabd* fails to teach or suggest the added claim limitation. Column 4, lines 42 – 44 and 49 – 54 of the *Elabd* reference states “Each row of data transferred from storage register 33 to transfer registers 17A and 17B is divided up between the two transfer registers 17A and 17B...In both transfer registers 17A and 17B an ‘empty site’ occurs in storage locations interleaved between charge values transferred from image array 13. The data held in transfer registers 17A and 17B are then clocked out through output ports 19A and 19B, respectively.” (Emphasis added). Accordingly, *Elabd* absolutely fails to teach or suggest Applicant’s invention, exemplarily disclosed in Figure 5, which requires at least two transfer registers which receive and concurrently transfer signal charges from at least two rows of pixels of said sensor array.

In light of the foregoing, Applicants submit that 35 U.S.C. §102 rejection must be withdrawn, and claims 1 – 8, 11, and 12 placed in condition for allowance.

B. The §103 Prior Art Rejections are Improper

Applicants respectfully request reconsideration of the Examiner’s rejection of claims 9, 10, 13, and 14 under 35 U.S.C. §103(a). Examiner has rejected these claims in view of the cited prior art reference of *Elabd et al.* (U.S. Patent No. 5,196,939) and further in view of *Kokudo* (U.S. Patent No. 5,298,734) or *Hirmada* (U.S. Patent No. 6,028,299).

Under Section 2143 of the MPEP, in order to establish a prima facie case of obviousness, the Examiner must meet three basic criteria. “First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference

teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.” *MPEP* §2143 rev. 3 (August, 2005). Applicants assert that the Examiner has failed to establish a prima facie case of obviousness for at least the reason that the prior art references, even if combined, fail to teach or suggest **all** of the claim limitations.


As discussed above, *Elabd* fails to teach or suggest wherein said plurality of transfer registers includes **two** transfer registers which receive and concurrently transfer signal charges from at least **two** rows of pixels of said sensor array. Applicants submit that neither one of the *Kokudo* or *Hirmada* references make up for this deficiency.

In light of the foregoing, Applicants submit that 35 U.S.C. §103 rejections must be withdrawn, and claims 9, 10, 13, and 14 placed in condition for allowance.

Respectfully submitted,

Date:

12/15/05


(Reg. #37,607)

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